PRACTICAL SUMMER TRAINING

Undertaken at

DEFENCE LABROATORY

DEFENCE RESEARCH & DEVELOPMENT ORGANISATION

JODHPUR – 342 011

Training on "*Control of 16 devices through a digital keypad*"

ABOUT DEFENCE LABORATORY, JODHPUR

Defence Laboratory, Jodhpur was established on 16th May, 1959. DLJ is located at the gateway of Thar Desert of Rajasthan. It enhances the operational efficiency of troops in desert warfare and logistics support. The aim of the lab is to undertaken research studies in the following areas:

- Camouflage & Low Observable Devices
- Nuclear Radiation Management & Applications
- Desert Environmental Science & Technologies

In addition to R&D activities in the above field, the lab conducts several training programs to the benefit of Services and Civil population, e.g. industrial radiography, NBC, radiation safety aspects, water desalination, quality, monitoring and desert meteorology. The lab has also been identified as a nodal agency by Inter Services Camouflage and Deception committee, army HQ for research, design, development and fabrication of deception devices and decoys for the three Services.

It may also be mentioned that the lab provides consultancy to the Services in the areas of non-destructive testing, radio isotopic applications, water problems and camouflage. The lab is also actively involved as work centre in giving technical support to major DRDO programs like Prithvi, SFD, LCA, MBT Arjun, INSTEP etc. Logistic and administrative support is given for demonstrations and trials in Pokharan and Mahajan Ranges organized by sister labs. The lab is also undertaking Societal Mission Activities based on S&T technologies developed by the lab for providing safe drinking water in hard core villages of Barmer, Rajasthan under project "SUJALAM" and to earthquake/cyclone affected areas under disaster management requirement of government of India.

SCOPE OF TRAINING

Practical Training is an important constituent of any curriculum and the B.E. course is no exception to this general rule. A practical training helps a student in getting acquainted with the manner in which his knowledge in being practically used outside his institute and this is normally different from what he has learnt from books. Hence, when one switches from the process of learning to that of implementing his knowledge he finds an abrupt change. This is exactly why Practical Training session during the B.E. curriculum becomes all the more important.

The duration of the Practical Training period prescribed for awarding the B.E. degree, is 90 days in our college. This period has been divided in two parts via a 45 days Practical Training after the 2nd.year B.E. session and a 45 days Practical Training after the 3rd.year B.E. session.

This report describes in detail my training after the 2nd year B.E. session, which I completed at the DLJ, The training was in designing of digital electronic circuits.

LEARNING OBJECTIVES

SHORT TERM

In this time period we were given instructive training about device control and their stimulation. We were also told to prepare an abstract on any new technology. In which I prepare a project on control of device with less wire. This report was submitted to them. They also told us how device are controlled at a Remote area and the operator operates it via a key board or any device. In this I learn the application of digital electronics up to an extent.

LONG TERM

In long term period we were told to prepare a project report on control of 16 devices via 4*4 keyboard. So I have prepared my report on control of 16 devices via 4*4 keyboard and given to the director of DRDO, Jodhpur.With the help of reference books, research paper in the defence lab and different websites. Being a student of electronics it enhanced my knowledge about the various electronic equipments which help in the long-term.

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OBJECT: DESIGN AN ELECTRONIC DIGITAL CIRCUIT FOR "CONTROL OF 16 DEVICES THROUGH A DIGITAL KEYPAD"

CIRCUIT DESCRIPTION:

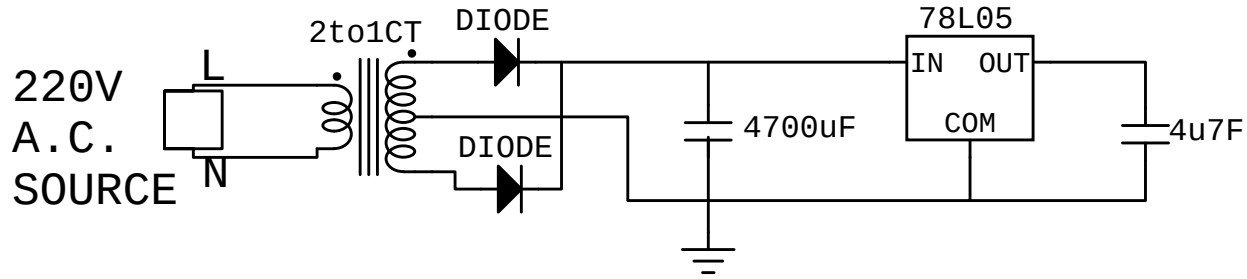
The circuit can be divided into 4 parts:

(1) Rectifier circuitry

(2) Keypad circuitry
(3) Clock and counter circuitry
(4) Device Driver Circuitry

***(1)** RECTIFIER CIRCUITRY:*

The rectifier circuitry is consisting of the 9-0-9volt, 250mA step down transformer takes 220V 50Hz A. C. Input in the primary winding and convert it into 9 volt A.C supply. The secondary winding of the transformer is center tapped, and it is used in full wave rectifier circuit. At the first and third nodes of the transformer, two 1N4007 diodes are employed to rectify A. C.; both the outputs of diodes are made one terminal by shorting them. This single terminal is used as positive terminal. The second node is used as negative or ground terminal. A capacitor valued 4700 microfarad is connected in parallel with output of transformer as a shunt capacitor filter. After this capacitor, a regulator IC7805 is employed which gives 5V regulated output. Then a capacitor of value 4.7 microfarad is connected to remove the remaining ripples from the D.C. output. Thus the 5V output is get, which can now be used wherever required, as +V and ground.



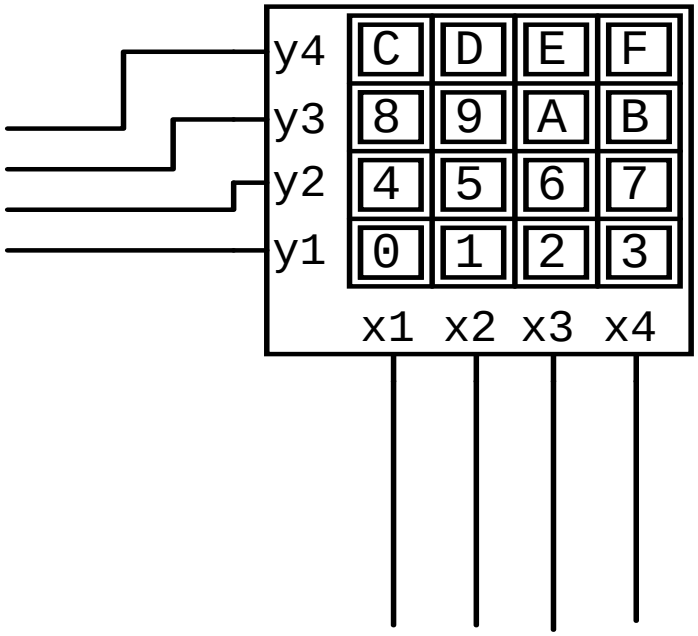
(2)** KEYPAD CIRCUITRY**:

Keypad circuitry consists of 16, PCB mounted type press to ON switches. The switches are arranged in 4 * 4 matrixes. In this matrix the ‘0’ output is get at (4, 1) position and it increases as 1, 2, 3 in right side. Then ‘4’ output is get at (3, 1) and it increases as 5, 6, 7 in right side. Then ‘8’ output is get at (2, 1) and it increases as 9, 10, 11 in right side. Then ‘12’ output is get at (1, 1) and it increases as 13, 14, 15 in right side.

This circuitry uses conventional hexadecimal symbols, in which A is used for 10, B is used for 11,C is used for 12, D is used for 13, E is used for 14, F is used for 15.

All the rows are fed from 4 outputs of IC74LS139 and all the columns get positive voltage from Vcc through resistors.

All the columns X1, X2, X3, X4 remains always high. After IC74LS75, IC74LS139 is employed, having dual decoders, which uses Q3 Q2 Q1 Q0 as input for A1a A0a (for second decoder) A1b A0b (for first decoder) and gives 8-bit Q3a Q2a Q1a Q0a Q3b Q2b Q1b Q0b (Y4 Y3 Y2 Y1 Z4 Z3 Z2 Z1) output. The four outputs Z1, Z2, Z3, Z4 are connected to four NOR gates.



The A0a, A1a, A0b, A1b both pairs gives 4-4 outputs.

(A).When A0a, A1a = 00, so Y1=0 and Y2, Y3, Y4=1

1) When A0b, A1b = 00, so Z1 will be low and if user presses ’0’, first NOR gate will be enabled & clock pulse will be generated.
2) When A0b, A1b = 01, so Z2 will be low and if user presses ’1’, second NOR gate will be enabled & clock pulse will be generated.
3) When A0b, A1b = 10, so Z3 will be low and if user presses ’2’, third NOR gate will be enabled & clock pulse will be generated.
4) When A0b, A1b = 11, so Z4 will be low and if user presses ’3’, fourth NOR gate will be enabled & clock pulse will be generated.

(B).When A0a, A1a = 01, so Y2=0 and Y1, Y3, Y4=1

1) When A0b, A1b = 00, so Z1 will be low and if user presses ’4’, first NOR gate will be enabled & clock pulse will be generated.

2) When A0b, A1b = 01, so Z2 will be low and if user presses ’5’, second NOR gate will be enabled & clock pulse will be generated.
3) When A0b, A1b = 10, so Z3 will be low and if user presses ’6’, third NOR gate will be enabled & clock pulse will be generated.
4).When A0b, A1b = 11, so Z4 will be low and if user presses ’7’, fourth NOR gate will be enabled & clock pulse will be generated.

(C). When A0a, A1a = 10, so Y3=0 and Y2, Y1, Y4=1

1) When A0b, A1b = 00, so Z1 will be low and if user presses ’8’, first NOR gate will be enabled & clock pulse will be generated.
2) When A0b, A1b = 01, so Z2 will be low and if user presses ’9’, second NOR gate will be enabled & clock pulse will be generated.
3) When A0b, A1b = 10, so Z3 will be low and if user presses ’10’, third NOR gate will be enabled & clock pulse will be generated.

4) When A0b, A1b = 11, so Z4 will be low and if user presses ’11’, fourth NOR gate will be enabled & clock pulse will be generated.

(D). When A0a, A1a = 11, so Y4=0 and Y2, Y3, Y1=1

1) When A0b, A1b = 00, so Z1 will be low and if user presses ’12’, first NOR gate will be enabled & clock pulse will be generated.
2) When A0b, A1b = 01, so Z2 will be low and if user presses ’13’, second NOR gate will be enabled & clock pulse will be generated.
3) When A0b, A1b = 10, so Z3 will be low and if user presses ’14’, third NOR gate will be enabled & clock pulse will be generated.
4) When A0b, A1b = 11, so Z4 will be low and if user presses ’15’, fourth NOR gate will be enabled & clock pulse will be generated.

All 4 outputs of NOR gates are O Red by 4 parallel diodes. The O Red output is used as clock pulse for IC74LS175.

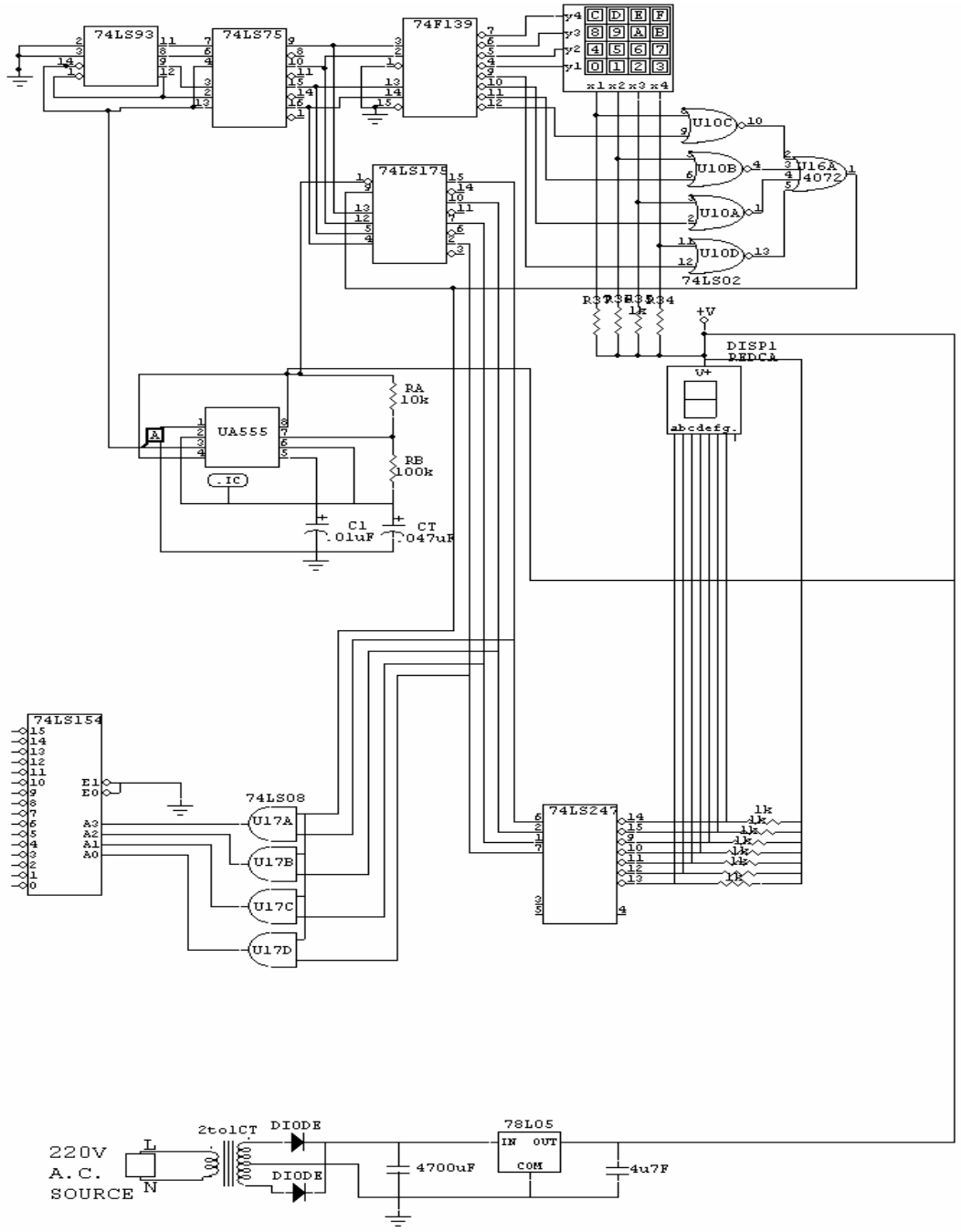
(3) *CLOCK AND COUNTER CIRCUITRY****:***

In this circuit, IC555 is a widely used timer IC that is used as a clock pulse generator (oscillator). When 5V signal is applied, a continuous square wave of constant amplitude (5V) and frequency is generated and can be get at pin 3. Now, IC74LS93 is a binary counter in which output of IC555 and Q0 output of IC74LS93 are feedback as clock pulses. The output is BCD at Q3 Q2 Q1 Q0. IC74LS75 consists of 2 –pairs of D-flip flops. Input is Q0 Q1 & Q2 BCD at Q3 Q2 Q1 Q0. This IC acts as a buffer and when clock becomes high all the BCD data at input is transferred to output.

Between IC74LS75 and IC74LS139, two wires are excluded; by which the output BCD is fed to 4 D-flip flops of IC74LS175. Whenever clock becomes high, the data at D-inputs is transferred to Q0 Q1 Q2 Q3.The output drives 2 paths. At first path, output is sent into 7-segment driver IC74LS47, which decodes the BCD into 7-segment output, followed by 7-segment display.

(4) *DEVICE DRIVER CIRCUITRY****:***

At second path, BCD output is fed into IC74LS08, consisting of 4 AND gates. The one input in all AND gates is connected to the clock pulse of IC74LS175, because here the requirement is to synchronize the inputs of IC74154 with clock and the remaining 4 inputs are BCD outputs. The 4 outputs of AND gates is connected to 4-line to 16-line decoder IC74LS154. THIS IC has four selection terminals which control the 16 terminal on which 16different equipment can place and their switching is controlled.



WORKING OF THE CIRCUIT:

Working of this circuit can be divided into 4 parts:

(1) Rectifier circuitry.
(2) Clock and counter circuitry.
(3) Keypad circuitry.
(4) Device driver circuitry.

***(1)** Rectifier circuitry:*

When the supply is switched ON, the transformer converts 230V A.C. into

6-0-6 A.C. Further this voltage is rectified through diodes and filtered by capacitor. This D.C. voltage fed to 3 terminal regulator to convert D.C. voltage into 5V regulated.

(2) *Clock and counter circuitry.*

In this circuitry, a 555 timer IC used in Astable multivibrator configuration. It's output square clock pulses fed to a BCD counter the BCD output, further send to a four flip-flops data transfer IC so that the BCD output of the counter, is latched at output of it. This BCD out put then fed to D type FF and keypad circuit .The output of DFF sends to display and rely driver circuit when any key is pressed.

(3) *Keypad circuitry:*

A keypad circuitry is a circuit, which gives it's output in BCD form, which is equivalent to the particular key pressed. In this circuit, a dual 2-to-4 decoder IC, a 16 key keypad, quad NOR gate and D FF are used in such a manner so that we can achieve desired output. Below a table shows different output on pressing different key's (see circuit diagram).

S. No	BCD	Key No.	Y 1	Y2	Y 3	Y 4	Z 1	Z 2	Z 3	Z 4	KEY NO. PRESSED	OUTPUT
1	0000	0	0	1	1	1	0	1	1	1	0	'HIGH' elselow
2	0001	1	0	1	1	1	1	0	1	1	1	'HIGH' elselow
3	0010	2	0	1	1	1	1	1	0	1	2	'HIGH' elselow
4	0011	3	0	1	1	1	1	1	1	0	3	'HIGH' elselow
5	0100	4	1	0	1	1	0	1	1	1	4	'HIGH' elselow
6	0101	5	1	0	1	1	1	0	1	1	5	'HIGH' elselow
7	0110	6	1	0	1	1	1	1	0	1	6	'HIGH' elselow
8	0111	7	1	0	1	1	1	1	1	0	7	'HIGH' elselow
9	1000	8	1	1	0	1	0	1	1	1	8	'HIGH' elselow
10	1001	9	1	1	0	1	1	0	1	1	9	'HIGH' elselow
11	1010	10	1	1	0	1	1	1	0	1	10	'HIGH' elselow
12	1011	11	1	1	0	1	1	1	1	0	11	'HIGH' elselow
13	1100	12	1	1	1	0	0	1	1	1	12	'HIGH' elselow
14	1101	13	1	1	1	0	1	0	1	1	13	'HIGH' elselow
15	1100	14	1	1	1	0	1	1	0	1	14	'HIGH' elselow
16	1111	15	1	1	1	0	1	1	1	0	15	'HIGH' elselow

(4) *Device driver circuitry:*

Human tendency of pressing a switch is dissimilar with everyone. This type of delay in releasing switch can generate another clock pulse, which will certainly disable the device, and just a quick flash of the device will be encountered there.

To compensate such problems, a monoshot is employed which disables the clock circuitry for an approximate period of 0.5 second.

AND gates are employed in the circuit to send BCD input to the 4-to-16 decoder momentarily so that corresponding to the BCD, the output of decoder also active momentarily.

The output of decoder serves as a clock pulse for J K flip-flop, so the corresponding flip-flop toggles and according to the output of flip-flop the corresponding relay becomes ON or OFF.

INTRODUCTION TO INTEGRATED CIRCUITS (IC'S)

Digital design is concerned with the design of digital electronic circuits. Digital circuits are employed in the design and construction of systems such as computers, data communications, Digital recording, Device handling, and many other applications.

An IC is just a packaged electronic circuit. A more detailed definition is: "An IC is a complete electronic circuit in which both the active and passive components are fabricated on an extremely tiny single chip of silicon**.**

ADVANTAGES OF IC's:

1. Extremely small physical size.
2. Very small weight.
3. Reduced cost.
4. Extremely high reliability.
5. Suitability for small-signal operation.
6. Low power consumption.
7. Easy replacement.

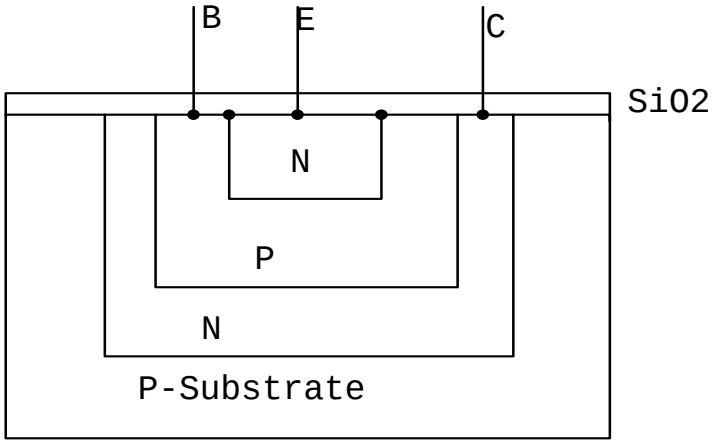
DRAWBACKS OF IC's :

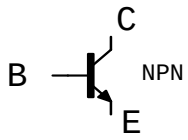
1. Coils or inductors cannot be fabricated.
2. IC's function at fairly low voltages.
3. They handle only limited amount of power.
4. They are quite delicate and cannot withstand rough handling or excessive heat.

However, the advantages of IC's far outweigh their disadvantages or drawbacks.

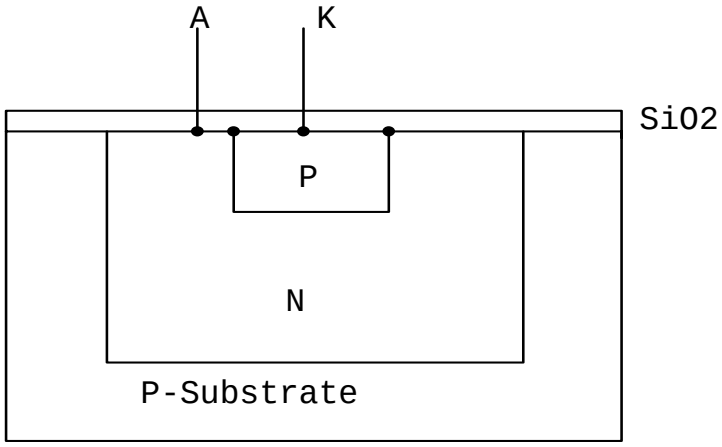
FABRICATION OF IC COMPONENTS

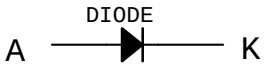
1. *TRANSISTOR*



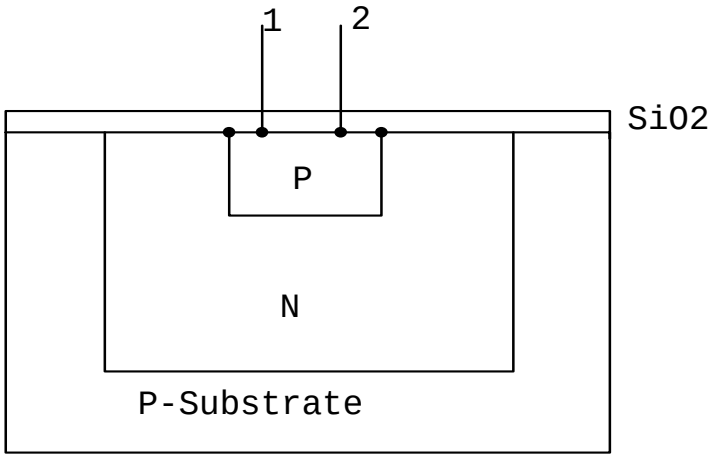


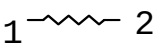
2. *DIODE*



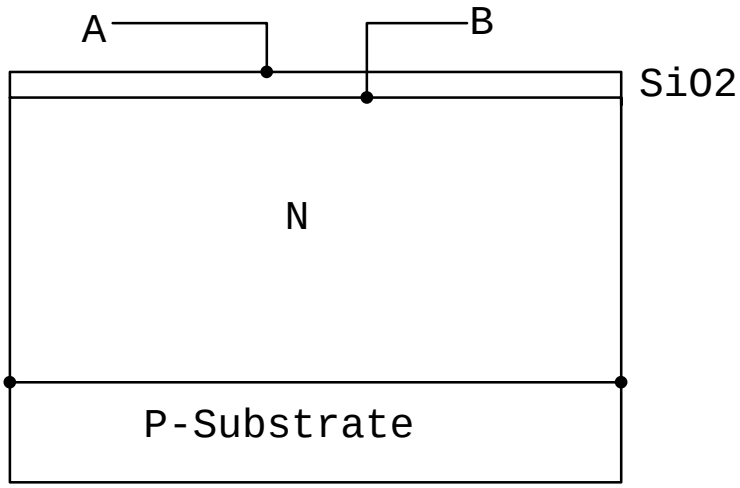


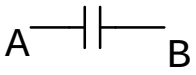
3. *RESISTOR*





4. *CAPACITOR*





DESCRIPTION OF COMPONENTS:

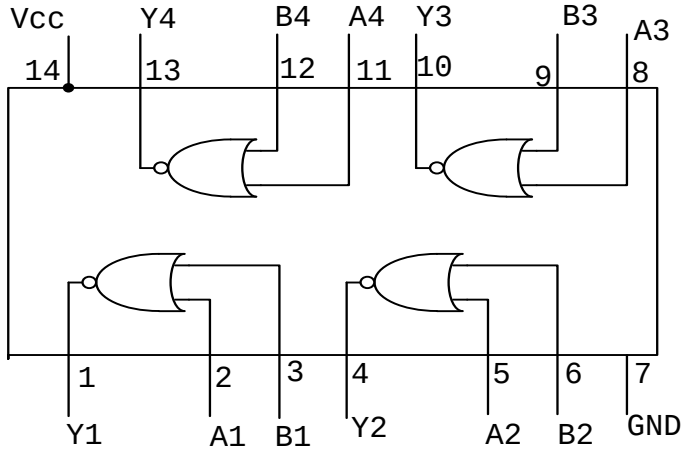
1. DM74LS02

QUAD 2-INPUT NOR GATE

The 74LS02 contains four independent gates each of which perform the logic NOR function. If we have a look upon the truth table of NOR gate, we find that NOR gate gives HIGH output, only when both the inputs are low.

Both NOR and NAND gates are called as "UNIVERSAL GATES", because the other gates can be derived from them.

CONNECTION DIAGRAM: Dual – in – Line Package



FUNCTION TABLE: Y = (A + B)' H = High Logic Level
L = Low Logic Level

INPUTS		OUTPUTS
A	B	Y

L	L	H
L	H	L
H	L	L
H	H	L

ABSOLUTE MAXIMUM RATINGS

The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" Table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

1. Supply-voltage 7volt
2. Input-voltage 7volt
3. Operating Free Air Temperature Range
   DM74LS02 0^0 C to $+70^0$ C
4. Storage Temperature- Range -65^0 C to $+150^0$ C

2. DM74L2S47

BCD TO 7-SEGMENT DRIVER

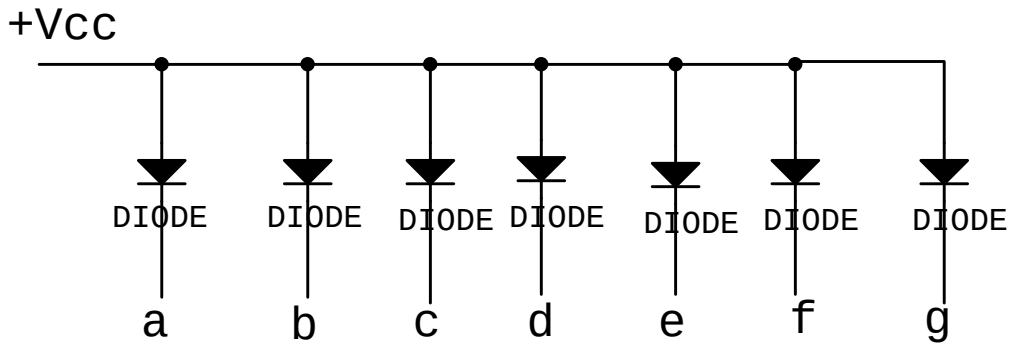
The 74LS47 accepts four lines of BCD (8421) input data, generates their complements internally and decodes the data with seven AND/OR gates having open collector outputs. To drive seven segments indicator directly.

A LED emits radiation when forward-biased, because free electrons recombine with holes near the junction. As the free electrons fall from a higher energy level; to a lower one, they give up energy in the form of heat & light. By using elements like Gallium, Arsenic and Phosphorous etc. a LED emits red, green, yellow, blue, orange and infra-red (invisible) light. LEDs that produce visible radiation are useful in test instruments, pocket calculators etc.

In the seven segment indicators LEDs are labeled from a to g.
Seven segment indicators are of 2 types:

1. *COMMON ANODE TYPE:*

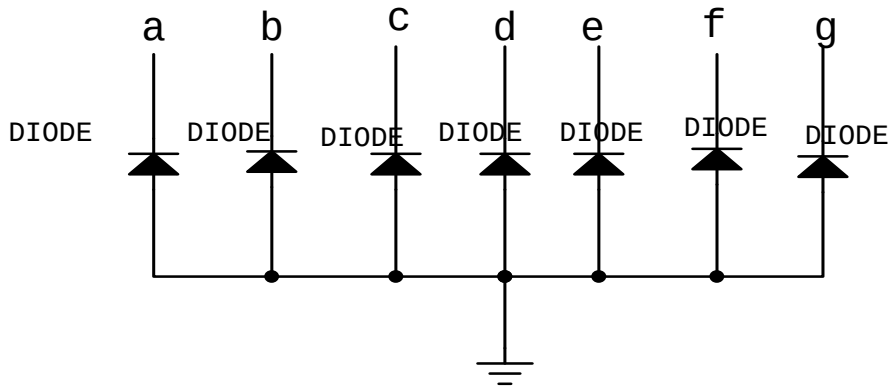
All anodes are connected together. A current limiting resistor is connected between each LED and GROUND. The size of this resistor determines how much current flow through the LED.



2. COMM ON

CATHODE TYPE:

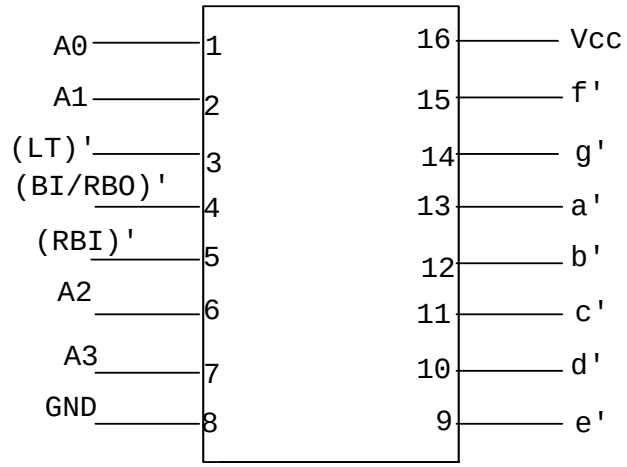
All cathodes are connected together. A current limiting resistor is connected between each LED and Vcc. The size of this resistor determines how much current flow through the LED.



FEATURES:

1. Open-collector outputs
2. Drive indicator segments directly

CONNECTION DIAGRAM: Dual – in – Line Package



Pin Names	Description
A0-A3	BCD Inputs
(RBI)’	Ripple Blanking Input (Active LOW)
(LT)’	Lamp Test Input (Active LOW)
(BI/RBO)’	Blanking Input (Active LOW) or Ripple Blanking Output (Active LOW)
A’-g’	Open Collector Segment Outputs (Active LOW)

ABSOLUTE MAXIMUM RATINGS

The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the “Electrical Characteristics” Table are not guaranteed at the absolute maximum

ratings. The “Recommended Operating Conditions” table will define the conditions for actual device operation.

1. Supply-voltage 7volt
2. Input-voltage 7volt
3. Operating Free Air Temperature Range
   DM74LS47 0^0 C to $+70^0$ C
4. Storage Temperature- Range -65^0 C to $+150^0$ C

FUNCTION DESCRIPTION

The LS47 decodes the input data in the pattern indicated in the truth table and the segment identification illustration. If the input data is decimal zero, a LOW signal applied to the (RBI)’ blanks the display and causes a multi-digit display. For example, by grounding the (RBI)’ of the highest order decoder and connecting its (BI/RBO)’ to (RBI)’ of the next lowest order decoder, etc., leading zeros will be suppressed. Similarly, by grounding (RBI)’ of the lowest order decoder and connecting its (BI/RBI)’ to (RBI)’ of the next highest order decoder, etc., trailing zeroes can be suppressed. Leading and trailing zeros can be suppressed simultaneously by using external gates, i.e.: by driving (RBI)’of a intermediate decoder from an OR gate whose inputs are (BI/RBI)’of the next highest and lowest order decoders. (BI/RBI)’ also serves as an unconditional blanking input. The internal NAND gate that generates the (RBI)’ signal has a resistive pull-up, as opposed to a totem pole, and thus (BI/RBI)’ can be forced LOW by external means, using wired-collector logic. A LOW signal thus applied to (BI/RBI)’ turns off all segment outputs. This blanking feature can be used to control display intensity by varying the duty cycle of the blanking signal. A LOW signal applied to (LT)’ turns on all segment outputs, provided that (BI/RBI)’ is not forced LOW.

TRUTH TABLE

Decimal Or Function	Inputs							Outputs							Note
	LT	RBI’	A3	A2	A1	A0	BI/RBO	a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	1
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	1
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
BI	X	X	X	X	X	X	L	H	H	H	H	H	H	H	2

RBI	H	L	L	L	L	L	L	H	H	H	H	H	H	H	3
LT	L	X	X	X	X	X	H	L	L	L	L	L	L	L	4

Note 1: (BI/RBO)' is wire-AND logic serving as blanking input (BI) and/or Ripple-Blanking output (RBO)'. The blanking out (BI)' must be Open or held at a HIGH Level when output functions 0 through 15 are desired, and ripple-blanking input (RBI)' must be open or At a HIGH level if blanking or a decimal 0 is not desired. X = Input may be HIGH or LOW.

Note 2: When a LOW level is applied to the blanking Input (forced Condition) all Segment outputs go to a HIGH level regardless of The state of any other input Condition.

Note 3: When ripple-blanking input (RBI)' and inputs A0, A1, A2, and A3 IS LOW Level, with the lamp test input at HIGH level, all Segment outputs go to a HIGH Level and the ripple blanking Output (RBI)' goes to a LOW level (Response condition).

Note 4: When the blanking input/ripple-blanking output (BI/RBO)' is open Or held at a HIGH level, and a LOW level is applied to lamp test Input, all segment outputs go to a LOW level.

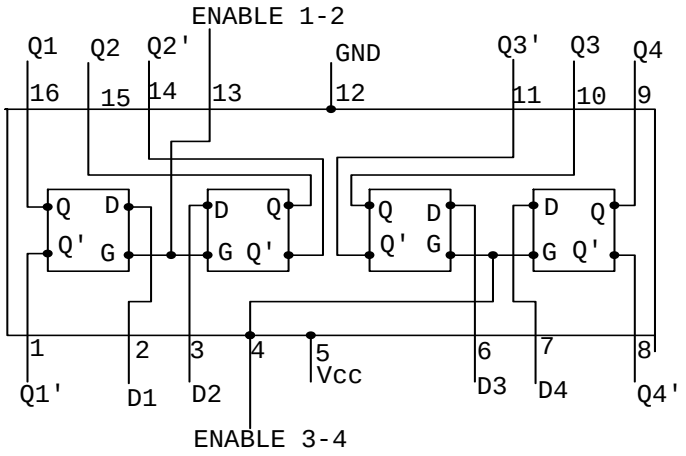
3.DM74LS75

QUAD LATCHES

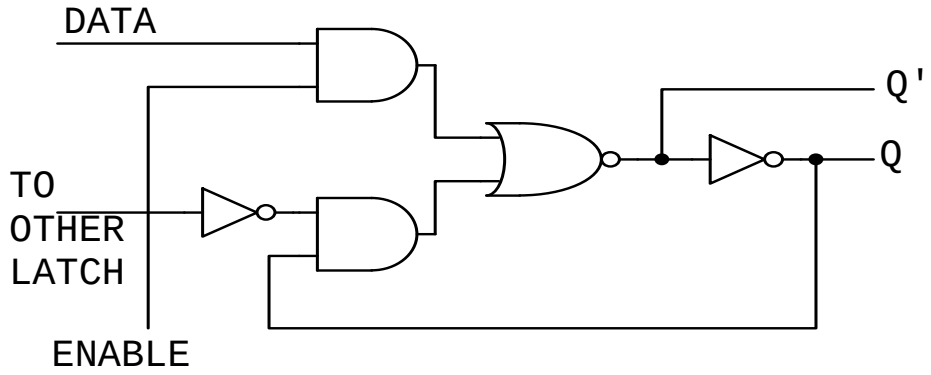
This latch is ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable is high, and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

This latch feature complementary Q and Q' outputs from a 4-bit latch, and are available in 16-pin packages.

CONNECTION DIAGRAM: Dual – in – Line Package



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUTS	
D	ENABLE	Q	Q’
L	H	L	H
H	H	H	L
X	L	Q0	Q0’

H = High Level, L = Low Level, X = don’t care
Q0 = the Level of Q before the High-to-Low Transition of ENABLE.

ABSOLUTE MAXIMUM RATINGS

The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the “Electrical Characteristics” Table are not guaranteed at the absolute maximum ratings. The “Recommended Operating Conditions” table will define the conditions for actual device operation.

1. Supply-voltage 7volt
2. Input-voltage 7volt

3. Operating Free Air Temperature Range
   DM74LS75 0^0 C to $+70^0$ C
4. Storage Temperature- Range -65^0 C to $+150^0$ C

4. **DM74LS93**

BINARY COUNTER

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-eight for the 'LS93.
This counter has a gated zero reset for use in BCD nine's complement applications.
To use its maximum count length (four bit binary), the B input is connected to the QA output. The input count pulses are applied to input and the outputs are as described in the appropriate truth table. A symmetrical divide-by-ten count can be obtained from the 'LS93 counters by connecting the QD output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output QA.

Counters, when driven by a clock can be used to count the no. of clock cycles. There are basically two types of counters:

(1) Synchronous counter
(2) Asynchronous counter

(2) Asynchronous counter:

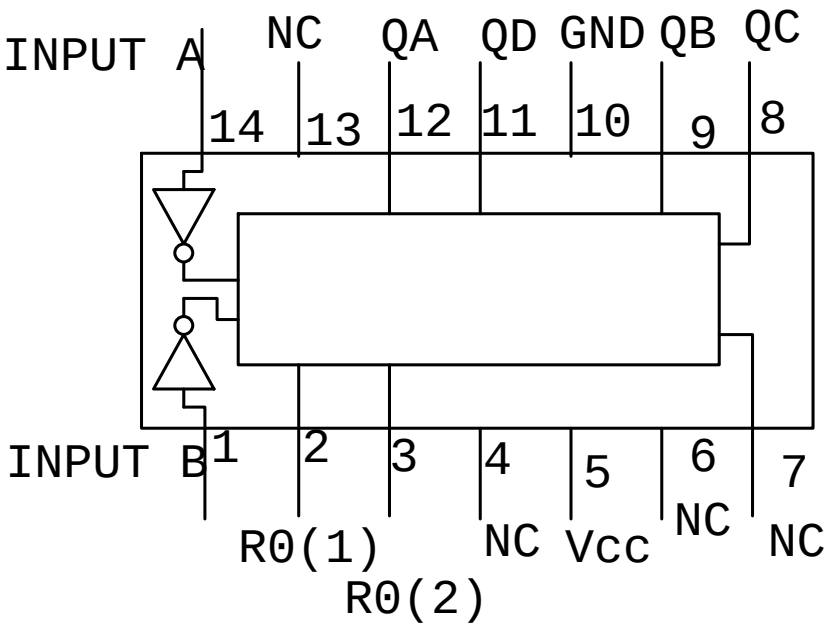
Each flip-flop is triggered by the previous flip-flop and thus the counter has a cumulative setting time. Since the triggers move through the flip-flops like a ripple in water, it is also known as ripple counter. Because of this the overall propagation delays time is the sum of the individual delays.

Every time there is a negative clock transition, first flip-flop will change state. Initially we assume all the flip-flops to be reset i.e. DCBA = 0000.

FEATURES

1. Typical power dissipation 45Mw
2. Count frequency 42 MHz

CONNECTION DIAGRAM: Dual – in –Line Package



ABSOLUTE MAXIMUM RATINGS:

The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits.

The parametric values defined in the "Electrical Characteristics" Table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

1. Supply-voltage 7volt
2. Input- voltage 7volt
3. Operating Free Air Temperature Range
   DM74LS93 0^0 C to $+70^0$ C
4. Storage Temperature- Range -65^0 C to $+150^0$ C

LS93 COUNT SEQUENCE

Count	Output			
	QD	QC	QB	QA
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L

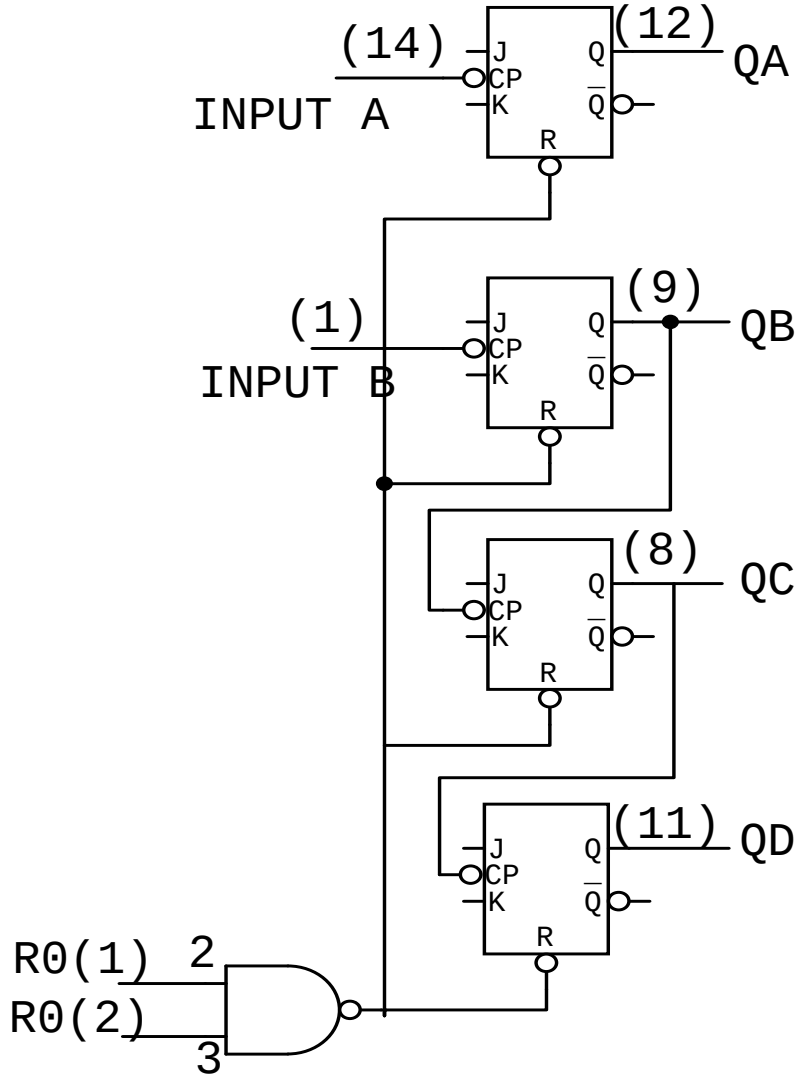
15	H	H	H	H

Note A: Output QA is connected to input B for BCD count.
Note B: Output QD is connected to input A for bi-quinary count.
Note C: Output QA is connected to input B.
Note D: H = High Level, L = Low Level, X = don't care.

LS93 RESET/COUNT TRUTH TABLE

Reset Inputs		Output			
R0(1)	R0(2)	QD	QC	QB	QA
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

LOGIC DIAGRAM



5. DM74LS139

DECODER

The LS139 comprises two separate two-line-to-four-line decoders in a single package. The entire decoder feature fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line ringing and simplify system design.

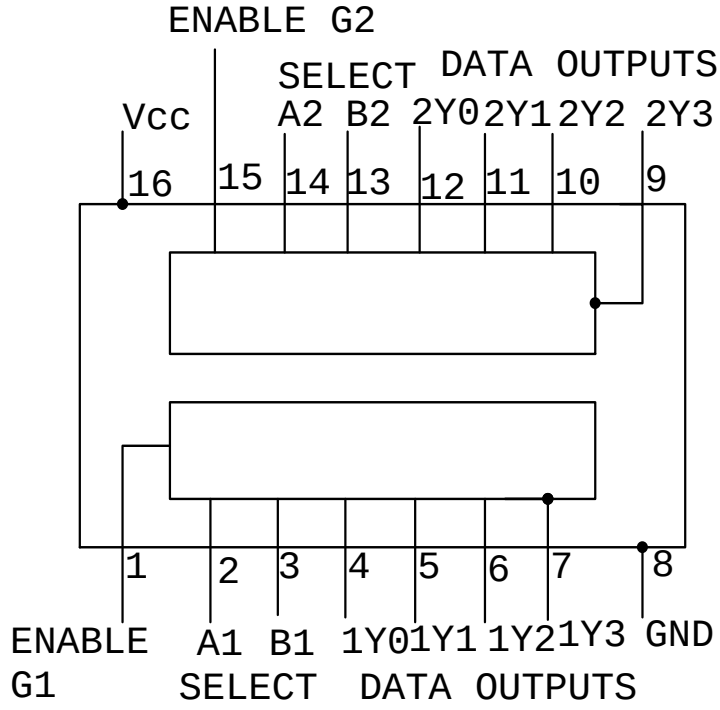
In the decoder, the ABCD are the control bits, when ABCD is 0001, only the Y1 AND gate has all inputs high, therefore only the Y1 output is high. If ABCD changes to 0100, only the Y4 AND gate has all inputs high; as a result, only the Y4 output goes high.

If we check the other ABCD possibilities, (0000 to 1111), we will find that the subscript of the high output always equals the decimal equivalent of ABCD.For this reason, the circuit is sometimes called a BINARY- TO – DECIMAL DECODER. Because it has 4 input lines and 16 output lines, the circuit is also known as a 4 LINE-TO-16 LINE DECODER.

FEATURES

1. LS139 contains two fully independent 2-to-4-line decoders.
2. Typical propagation delay (3 levels of logic)
   LS139 21ns
3. Typical power dissipation
   LS139 34Mw

CONNECTION DIAGRAM: Dual – in –Line Package



ABSOLUTE MAXIMUM RATINGS

The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" Table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

1. Supply-voltage 7volt
2. Input-voltage 7volt
3. Operating Free Air Temperature Range
   DM74LS139 0^0 C to $+70^0$ C

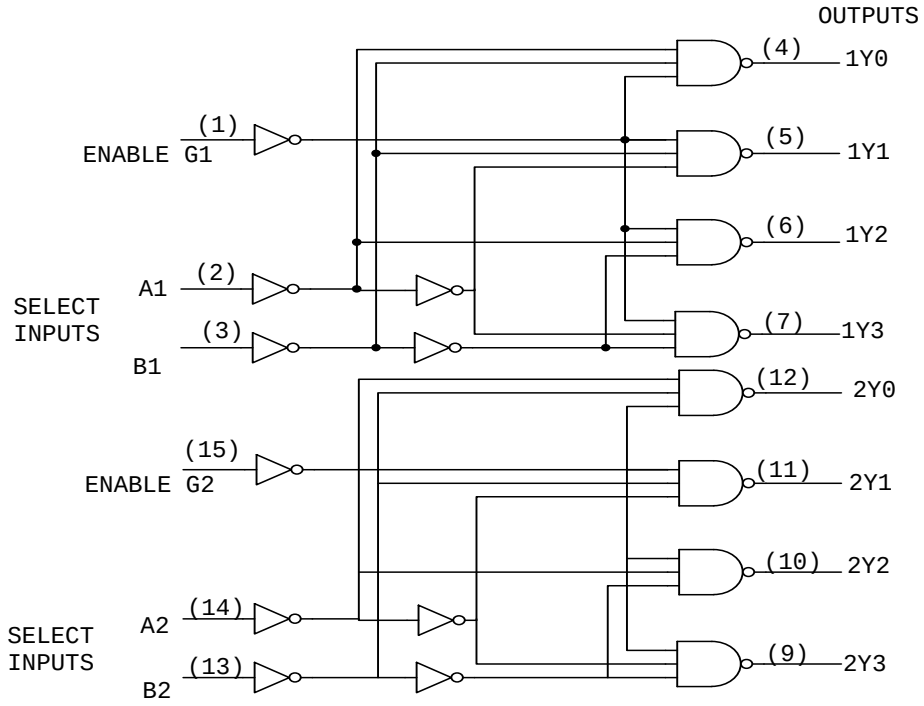
4. Storage Temperature- Range -65^0 C to $+150^0$ C

FUNCTION TABLE

INPUTS			OUTPUT			
ENABLE	SELECT					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = High Level, L = Low Level, X = don't care

LOGIC



6. DM74LS154

4-Line to 16-Line DECODER

Each of these 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. All inputs are buffered and input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design.

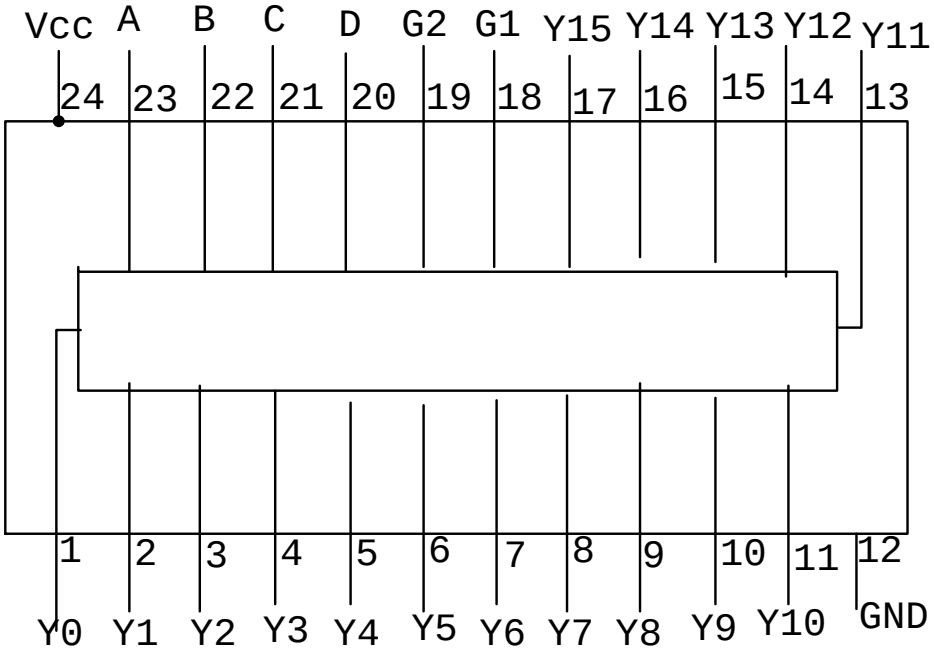
In the decoder, the ABCD are the control bits, when ABCD is 0001, only the Y1 AND gate has all inputs high, therefore only the Y1 output is high. If ABCD changes to 0100, only the Y4 AND gate has all inputs high; as a result, only the Y4 output goes high.

If we check the other ABCD possibilities, (0000 to 1111), we will find that the subscript of the high output always equals the decimal equivalent of ABCD.For this reason, the circuit is sometimes called a BINARY- TO – DECIMAL DECODER. Because it has 4 input lines and 16 output lines, the circuit is also known as a 4 LINE-TO-16 LINE DECODER.

FEATURES

1. Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs.
2. Input clamping diodes simplify system design.
3. High fan-out, low-impedance, totem-pole outputs.
4. Typical propagation delay 3 ns
   Levels of logic 23 ns
   Strobe 19 ns
5. Typical power dissipation 45mW.

CONNECTION DIAGRAM: Dual – in –Line Package



ABSOLUTE MAXIMUM RATINGS

The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" Table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

1. Supply-voltage 7volt
2. Input-voltage 7volt
3. Operating Free Air Temperature Range
   DM74LS154 0^0 C to $+70^0$ C
4. Storage Temperature- Range -65^0 C to $+150^0$ C

7. DM74LS175

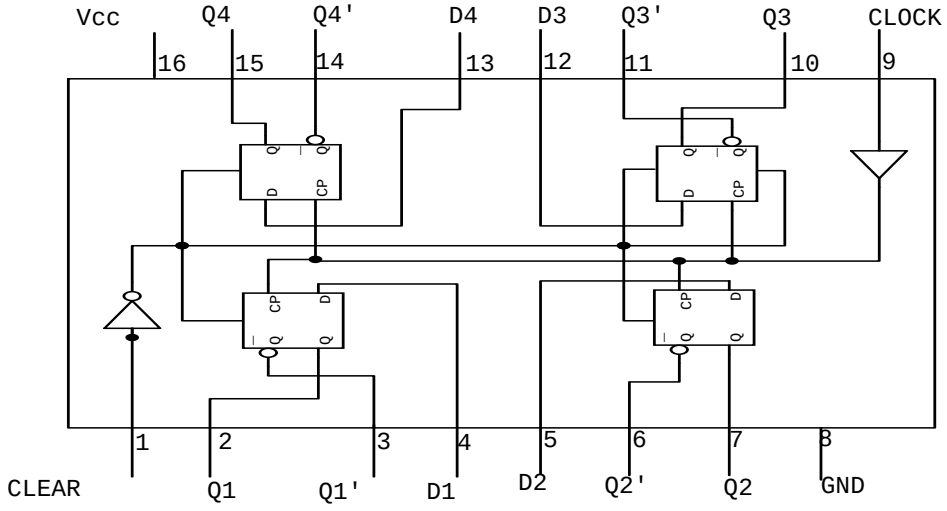
QUAD D-FLIP-FLOP WITH CLEAR

This positive edge triggered flip-flop utilizes TTL circuitry to implement D-type flip-flop logic. A direct clear input and the quad version feature complementary outputs from each flip-flop. Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive edge triggering occurs at a particular voltage level and is not directly related to the transition time of the positive going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

FEATURES

1. LS175 contains four flip-flops with double-real outputs.
2. Buffered clock and direct clear inputs.
3. Individual data input to each flip-flop.
4. Applications include:
   Buffer/storage registers
   Shift registers
   Pattern generators
5. Typical clock frequency 40MHz.
6. Typical power dissipation per flip-flop 14 mW.

CONNECTION DIAGRAM: Dual – in –Line Package



FUNCTION TABLE

Inputs			Outputs	
Clear	Clock	D	Q	Q’
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q0	Q0’

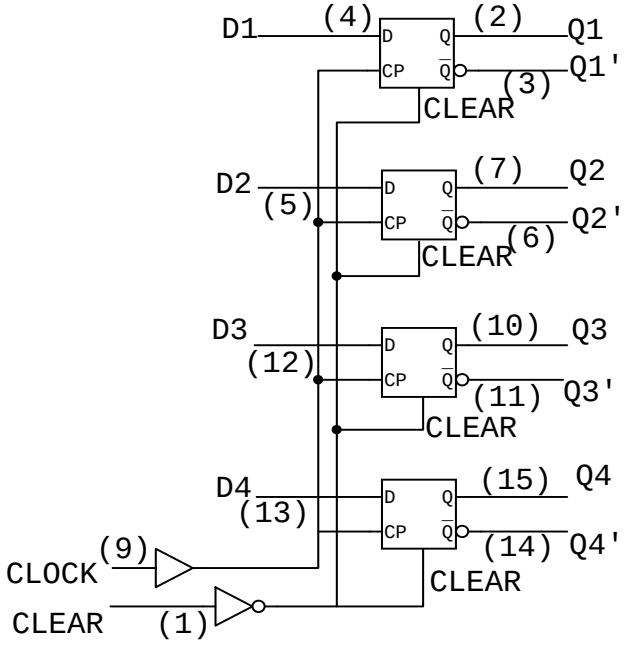
H = High Level (Steady State), L = Low Level (Steady State), X = don’t care
↑ = Transition from low to high level, Q0 = the level of Q before the Indicated steady-State Input conditions were established.

ABSOLUTE MAXIMUM RATINGS

The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the “Electrical Characteristics” Table are not guaranteed at the absolute maximum ratings. The “Recommended Operating Conditions” table will define the conditions for actual device operation.

1. Supply-voltage 7volt
2. Input-voltage 7volt
3. Operating Free Air Temperature Range
   DM74LS175 0^0 C to $+70^0$ C
4. Storage Temperature- Range -65^0 C to $+150^0$ C

LOGIC DIAGRAM

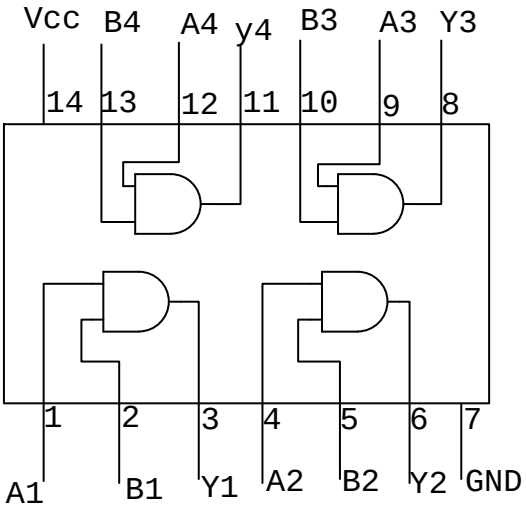


8. **DM74LS08**

QUAD 2-INPUT AND GATE

The LS08 contains four independent gates each of which perform the logic AND function. The AND gate gives HIGH output only when both the inputs are high.

CONNECTION DIAGRAM: Dual – in –Line Package



FUNCTION TABLE

Y = A*B H = High Logic Level
L = Low Logic Level

INPUTS		OUTPUTS
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

ABSOLUTE MAXIMUM RATINGS

The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" Table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

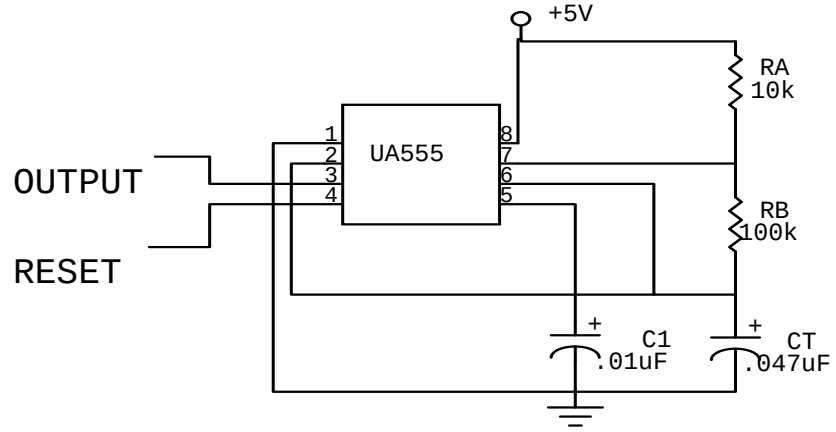
1. Supply-voltage 7volt
2. Input-voltage 7volt
3. Operating Free Air Temperature Range

DM74LS08	0^0 C to $+70^0$ C
4. Storage Temperature- Range	-65^0 C to $+150^0$ C

9. NE 555

The 555 timer is a highly stable integrated circuit capable of producing accurate time delays or oscillation. The frequency of oscillation and duty cycle are accurately controlled by only two external resistors and capacitor.

CONNECTION DIAGRAM



PIN DATA

PIN 1: GROUND terminal :It is a common ground terminal. All the voltages are measured with respect to this terminal.

PIN 2: TRIGGER terminal: The pin is an inverting input to comparator which is responsible for transition of flip-flop from set to reset. The output stage of timer depends on the amplitude of external trigger pulse applied to this pin.

PIN 3: OUTPUT terminal: Output of timer is available at this pin. Normally its level remains low and only during timing interval it goes high.

There are two pins ways to connect the load and only during timing interval it goes high.

PIN 4: RESET terminal: To disable or rest the timer a negative pulse is applied at this pin due to which it is called reset terminal. When this pin is not to be used for reset purpose, it should be connected to Vcc to avoid any possibility of false resetting.

PIN 5: CONTROL VOLTAGE terminal: Function of the control voltage terminal is to control the threshold and trigger level, and that's why this terminal is called control terminal.

PIN 6: THRESHOLD terminal: It is a noninverting terminal of comparator, which compares the voltage applied at this terminal with a reference voltage of +2Vcc/3.

PIN 7: DISCHARGE terminal: At this pin collector of a transistor is connected internally and mostly a capacitor connected externally between this terminal and ground. It is called discharge terminal because when transistor saturates, capacitor discharges through the transistor. When the transistor is cut off, the capacitor charges at a rate determined by external resistor and capacitor.

PIN 8:SUPPLY terminal: A supply voltage Vcc between +5V and +18V is applied to this pin with respect to ground. Due to such a large range of Vcc, existing digital logic supplies, linear IC supplies, and automobile or dry cell batteries can power 555.

APPLICATION OF TIMER AS AN AMV

An astable multivibrator has no stable state in output; therefore a media must be there for auto transition. In case of a 555 timer a capacitor is externally connected as this media to induce transition in both the logic states (high and low) of output by storing energy.

Charging time (T1) is given by equation $T1 = 0.693*(RA + RB) * C$.

Discharging time (T2) is given by equation $T2 = 0.693 * RB * C$.

Since total time period of output wave is $T = T1 + T2$

Therefore, $T = 0.693*(RA + RB) * C + 0.693 * RB * C.$

$= 0.693*(RA+2RB)*C.$

Thus frequency of oscillation is $f = 1 / T$

$= 1.44 / (RA+2RB)*C$

This equation indicates that frequency of oscillation in this AMV is independent of Vcc. To check the symmetry of output wave or to check the useful period of output wave duty cycle of output is determined. Duty cycle is ratio of time (T1) during which the output is high to the total time period T. Thus,

% duty cycle $= (T1 / T) *100$

$= [\{0.693*(RA+RB)*C\} / \{0.693*(RA+2RB)*C\}] *100$

$= \{(RA+RB) / (RA+2RB)\} * 100$

Depending on RA and RB the duty cycle lies between 50 and 100%.

COMPONENT USED: -

1. *PASSIVE COMPONENT*

a) RESISTANCE

10 K Ω- 1
100 K Ω - 1
4.7 K Ω - 8
1 KΩ - 7

b) CAPACITANCE

4700 μ_F - 1
47 μ_F - 1
4.7 μ_F - 1
0.01 μF - 1

2. *ACTIVE COMPONENT*

a) IC USED

74LS93
74LS75
74LS139
74LS175
74LS247
74LS02
74LS08
74LS154
40LS72
78L05

NE555

b) DIODE
1N 4007 – 2

c)7- SEGMENT DISPLAY

d) 16 MICRO SWITCH FOR MAKING OF 4*4 KEYPAD

3. *OTHERS*

9-0-9 CENTER TAP TRANSFORMER -1

ESTIMATE IN CONSTRUCTING PROJECT: - Rs. 600

ACHIEVEMENT

By this training we achieved how to overcome practical situation in real life and how to interact with people keeping ourselves calm and patient in our bad times too.

By this training we learned the whole procedure of device control where we theoretically and practically installed, commissioned and troubleshoot of these device and how these device are used in different fields. Thus we achieved the whole process in our valuable 45 days training.

The main achievement was being a part of an esteemed institute and of learning about the vast field of device control. Also we got the first task of working together in a fruitful learning environment.

CONCLUSION:

I would like to conclude this training as a very great and enriching experience to interact with the interesting field in the name of "DEVICE CONTROL AND STIMULATION".

During the training I familiarized myself with the use of P.C.B designing, application of I.C. its pin out diagram, construction of 4*4 keypad, construction of power supply and controlling the device by minimum no. of wires.

The circuit can be used in defence, industrial purpose as well as domestic purpose. In defence we can aim 16 different places to be exploded control by us at a remote place. Similarly we can use in domestic and industrial purpose by control maximum device via min. wires control at a remote area.

I also learned about the eng. Responsibility and about their hard work . this training was not only good for personality development but also great in terms of imparting practical knowledge .

Thus I conclude our training with a very nice and wonderful experience gained at DRDO, Jodhpur, under a peaceful kind and friendly environment.

BIBILIOGRAPHY:-

1. **DEFENCE LABORATORY Library.**
2. **DIGITAL CIRCUITS AND DESIGN- S.SALIVAHANAN**
3. **MODERN DIGITAL PRINCIPLES- R.K.JAIN**
4. **datasheetcatalogue**.com
5. **efy4u.com**